# AK4393

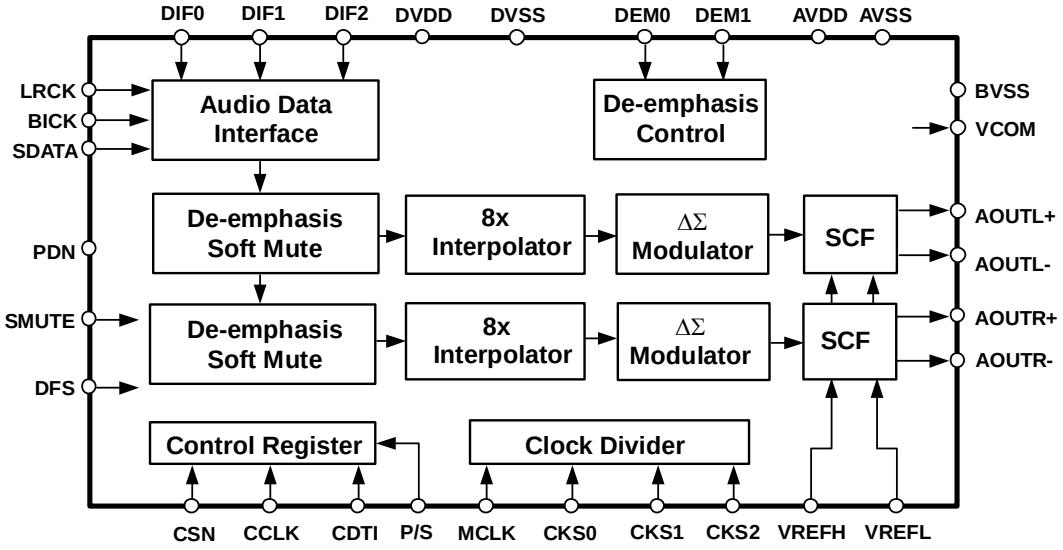
## Advanced Multi-Bit 96kHz 24-Bit ΔΣ DAC

### GENERAL DESCRIPTION

The AK4393 is a high performance stereo DAC for the 96kHz sampling mode of DAT, DVD including a 24bit digital filter. The AK4393 introduces the advanced multi-bit system for ΔΣ modulator. This new architecture achieves the wider dynamic range, while keeping much the same superior distortion characteristics as conventional Single-Bit way. In the AK4393, the analog outputs are filtered in the analog domain by switched-capacitor filter (SCF) with high tolerance to clock jitter. The analog outputs are full differential output, so the device is suitable for hi-end applications. The operating voltages support analog 5V and digital 3.3V, so it is easy to I/F with 3.3V logic IC.

### FEATURES

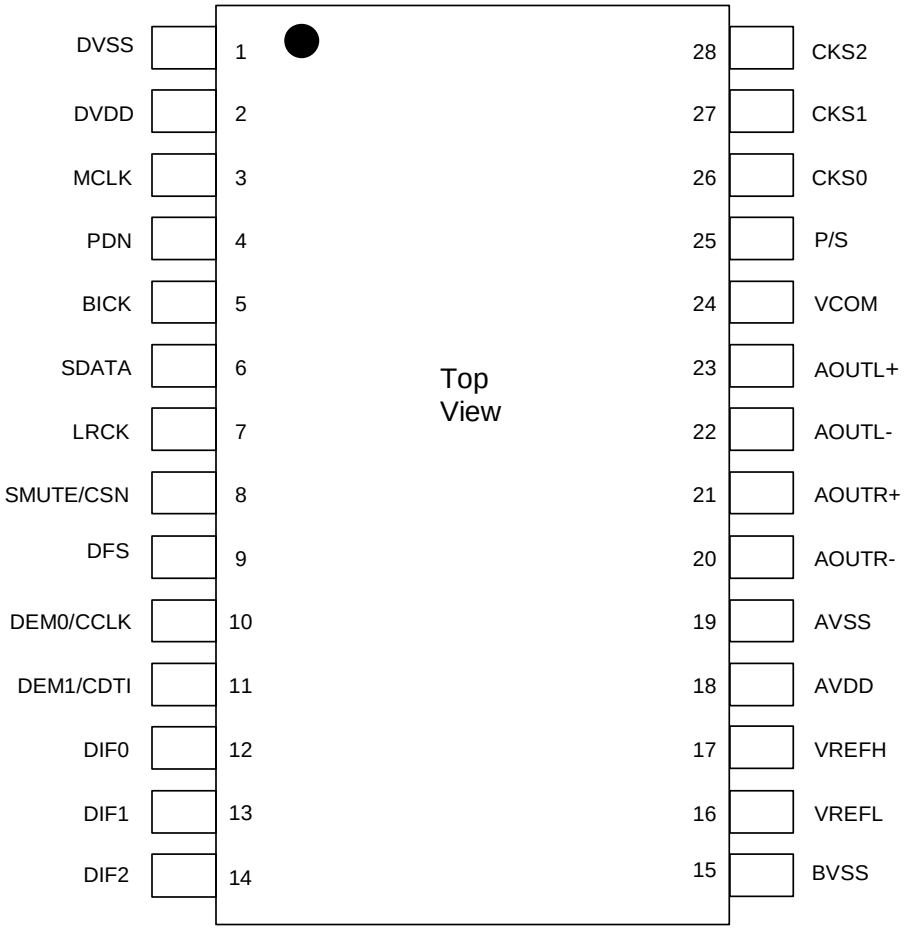
- **128x Oversampling**
- **Sampling Rate up to 108kHz**
- **24Bit 8x Digital Filter**
  **Ripple: ±0.005dB, Attenuation: 75dB**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **Digital de-emphasis for 32, 44.1, 48 & 96kHz sampling**
- **Soft Mute**
- **THD+N: -100dB**
- **DR, S/N: 120dB**
- **I/F format : MSB justified, 16/20/24bit LSB justified, $I^2S$**
- **Master Clock: Normal Speed: 256fs, 384fs, 512fs or 768fs**
  **Double Speed: 128fs, 192fs, 256fs or 384fs**
- **Power Supply: 4.75 to 5.25V (Analog), 3 to 5.25V (Digital)**
- **Small Package: 28pin VSOP**



## ■ Ordering Guide

| | | |
|---|---|---|
| AK4393VF | -40 ~ +85 °C | 28pin VSOP (0.65mm pitch) |
| AKD4393 | Evaluation Board | |

## ■ Pin Layout



## PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | DVSS | - | Digital Ground Pin |
| 2 | DVDD | - | Digital Power Supply Pin, 3.3V or 5.0V |
| 3 | MCLK | I | Master Clock Input Pin |
| 4 | PDN | I | Power-Down Mode Pin<br>When at "L", the AK4393 is in power-down mode and is held in reset.<br>The AK4393 should always be reset upon power-up. |
| 5 | BICK | I | Audio Serial Data Clock Pin<br>The clock of 64fs or more than is recommended to be input on this pin. |
| 6 | SDATA | I | Audio Serial Data Input Pin<br>2's complement MSB-first data is input on this pin. |
| 7 | LRCK | I | L/R Clock Pin |
| 8 | SMUTE | I | Soft Mute Pin in parallel mode<br>When this pin goes "H", soft mute cycle is initiated.<br>When returning "L", the output mute releases. |
| | CSN | I | Chip Select Pin in serial mode |
| 9 | DFS | I | Double Speed Sampling Mode Pin (Internal pull-down pin)<br>"L": Normal Speed , "H": Double Speed |
| 10 | DEM0 | I | De-emphasis Enable Pin in parallel mode |
| | CCLK | I | Control Data Clock Pin in serial mode |
| 11 | DEM1 | I | De-emphasis Enable Pin in parallel mode |
| | CDTI | I | Control Data Input Pin in serial mode |
| 12 | DIF0 | I | Digital Input Format Pin |
| 13 | DIF1 | I | Digital Input Format Pin |
| 14 | DIF2 | I | Digital Input Format Pin |
| 15 | BVSS | - | Substrate Ground Pin, 0V |
| 16 | VREFL | I | Low Level Voltage Reference Input Pin |
| 17 | VREFH | I | High Level Voltage Reference Input Pin |
| 18 | AVDD | - | Analog Power Supply Pin, 5.0V |
| 19 | AVSS | - | Analog Ground Pin, 0V |
| 20 | AOUTR- | O | Rch Negative analog output Pin |
| 21 | AOUTR+ | O | Rch Positive analog output Pin |
| 22 | AOUTL- | O | Lch Negative analog output Pin |
| 23 | AOUTL+ | O | Lch Positive analog output Pin |
| 24 | VCOM | O | Common Voltage Output Pin, 2.6V |
| 25 | P/S | I | Parallel/Serial Select Pin (Internal pull-up pin)<br>"L": Serial control mode, "H": Parallel control mode |
| 26 | CKS0 | I | Master Clock Select Pin |
| 27 | CKS1 | I | Master Clock Select Pin |
| 28 | CKS2 | I | Master Clock Select Pin |

Note: All input pins except internal pull-up/down pins should not be left floating.

## ABSOLUTE MAXIMUM RATINGS

(AVSS, BVSS, DVSS = 0V; Note 1)

| Parameter | | Symbol | min | max | Units |
|---|---|---|---|---|---|
| Power Supplies: | Analog | AVDD | -0.3 | 6.0 | V |
| | Digital | DVDD | -0.3 | 6.0 | V |
| | \| BVSS-DVSS \| (Note 2) | Δ GND | - | 0.3 | V |
| Input Current , Any pin Except Supplies | | IIN | - | ±10 | mA |
| Input Voltage | | VIND | -0.3 | DVDD+0.3 | V |
| Ambient Operating Temperature | | Ta | -40 | 85 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |

Notes: 1. All voltages with respect to ground.
2. AVSS, BVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(AVSS, BVSS, DVSS=0V; Note 1)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| Power Supplies: | Analog | AVDD | 4.75 | 5.0 | 5.25 | V |
| (Note 3) | Digital | DVDD | 3.0 | 3.3 | 5.25 | V |
| Voltage Reference | "H" voltage reference | VREFH | AVDD-0.5 | - | AVDD | V |
| (Note 4) | "L" voltage reference | VREFL | AVSS | - | - | V |
| | VREFH-VREFL | Δ VREF | 3.0 | - | AVDD | V |

Notes: 3. The power up sequence between AVDD and DVDD is not critical.
4. Analog output voltage scales with the voltage of (VREFH-VREFL).
AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = ±2.4Vpp×(VREFH-VREFL)/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

## ANALOG CHARACTERISTICS

(Ta = 25°C; AVDD = 5V, DVDD = 3.3V; AVSS, BVSS, DVSS = 0V, VREFH = AVDD, VREFL = AVSS;
fs = 44.1kHz; BICK = 64fs; Signal Frequency = 1kHz; 24bit Input Data; Measurement Bandwidth = 20Hz~20kHz;
$R_L \geq 600\Omega$; External circuit: Figure 11; unless otherwise specified)

| Parameter | | | min | typ | max | Units |
|---|---|---|---|---|---|---|
| Resolution | | | | | 24 | Bits |
| **Dynamic Characteristics** (Note 5) | | | | | | |
| THD+N | fs=44.1kHz | 0dBFS | | -100 | -90 | dB |
| | BW=20kHz | -60dBFS | | -53 | - | dB |
| | fs=96kHz | 0dBFS | | -97 | -86 | dB |
| | BW=40kHz | -60dBFS | | -51 | - | dB |
| Dynamic Range (-60dBFS with A-weighted) | fs=44.1kHz | (Note 6) | 112 | 117 | | dB |
| | | (Note 7) | - | 120 | | dB |
| | fs=96kHz | | 111 | 116 | | dB |
| | | (Note 7) | - | 118 | | dB |
| S/N (A-weighted | fs=44.1kHz | (Note 8) | 112 | 117 | | dB |
| | | (Note 7) | - | 120 | | dB |
| | fs=96kHz | | 111 | 116 | | dB |
| | | (Note 7) | - | 118 | | dB |
| Interchannel Isolation (1kHz) | | | 100 | 120 | | dB |
| **DC Accuracy** | | | | | | |
| Interchannel Gain Mismatch | | | | 0.15 | 0.3 | dB |
| Gain Drift | | (Note 9) | | 20 | - | ppm/°C |
| Output Voltage | | (Note 10) | ±2.25 | ±2.4 | ±2.55 | Vpp |
| Load Resistance | | (Note 11) | 600 | | | Ω |
| Output Current | | | | | 3.5 | mA |
| **Power Supplies** | | | | | | |
| Power Supply Current | | | | | | |
| Normal Operation (PDN = "H") | | | | | | |
| AVDD | | | | 60 | - | mA |
| DVDD(fs=44.1kHz) | | | | 3 | - | mA |
| DVDD(fs=96kHz) | | | | 5 | - | mA |
| AVDD + DVDD | | | | | 90 | mA |
| Power-Down Mode (PDN = "L") | | | | | | |
| AVDD + DVDD | | (Note 12) | | 10 | 50 | μA |
| Power Supply Rejection | | (Note 13) | | 50 | | dB |

Notes: 5. At 44.1kHz, measured by Audio Precision, System Two. Averaging mode.
At 96kHz, measured by ROHDE & SCHWARZ, UPD. Averaging mode.
Refer to the eva board manual.
6. 101dB at 16bit data and 116dB at 20bit data.
7. By Figure12. External LPF Circuit Example 2.
8. S/N does not depend on input bit length.
9. The voltage on (VREFH-VREFL) is held +5V externally.
10. Full-scale voltage (0dB). Output voltage scales with the voltage of (VREFH-VREFL).
AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = ±2.4Vpp×(VREFH-VREFL)/5.
11. For AC-load. 1kΩ for DC-load.
12. In the power-down mode. P/S = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held DVSS.
13. PSR is applied to AVDD, DVDD with 1kHz, 100mVpp. VREFH pin is held +5V.

## FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; fs = 44.1kHz; Normal Speed Mode; DEM = OFF)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Passband ±0.01dB (Note 14) | | PB | 0 | | 20.0 | kHz |
| -6.0dB | | | - | 22.05 | - | kHz |
| Stopband (Note 14) | | SB | 24.1 | | | kHz |
| Passband Ripple | | PR | | | ± 0.005 | dB |
| Stopband Attenuation | | SA | 75 | | | dB |
| Group Delay (Note 15) | | GD | - | 28 | - | 1/fs |
| **Digital Filter + SCF** | | | | | | |
| Frequency Response 0 ~ 20.0kHz | | | - | ± 0.2 | - | dB |

Note: 14. The passband and stopband frequencies scale with fs.
For example, PB = 0.4535×fs (@±0.01dB), SB = 0.546×fs.

15. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

## FILTER CHARACTERISTICS (fs = 96kHz)

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; fs = 96kHz; Double Speed Mode; DEM = OFF)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **Digital Filter** | | | | | | |
| Passband ±0.01dB (Note 14) | | PB | 0 | | 43.5 | kHz |
| -6.0dB | | | - | 48.0 | - | kHz |
| Stopband (Note 14) | | SB | 52.5 | | | kHz |
| Passband Ripple | | PR | | | ± 0.005 | dB |
| Stopband Attenuation | | SA | 75 | | | dB |
| Group Delay (Note 15) | | GD | - | 28 | - | 1/fs |
| **Digital Filter + SCF** | | | | | | |
| Frequency Response 0 ~ 40.0kHz | | | - | ± 0.3 | - | dB |

## DC CHARACTERISTICS

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| High-Level Input Voltage | | VIH | 70%DVDD | - | - | V |
| Low-Level Input Voltage | | VIL | - | - | 30%DVDD | V |
| Input Leakage Current | (Note 16) | Iin | - | - | ± 10 | μA |

Note: 16. DFS and P/S pins have internal pull-down or pull-up devices, nominally 100kΩ.

## SWITCHING CHARACTERISTICS

(Ta = 25°C; AVDD = 4.75~5.25V; DVDD = 3.0~5.25V; $C_L$ = 20pF)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Master Clock Timing** (Note 17) | | | | | |
| Normal Speed: 256fs, Double Speed: 128fs | fCLK | 7.7 | | 13.824 | MHz |
| Pulse Width Low | tCLKL | 28 | | | ns |
| Pulse Width High | tCLKH | 28 | | | ns |
| Normal Speed: 384fs, Double Speed: 192fs | fCLK | 11.5 | | 20.736 | MHz |
| Pulse Width Low | tCLKL | 20 | | | ns |
| Pulse Width High | tCLKH | 20 | | | ns |
| Normal Speed: 512fs, Double Speed: 256fs | fCLK | 15.4 | | 27.648 | MHz |
| Normal Speed: 768fs, Double Speed: 384fs | fCLK | 23.0 | | 41.472 | MHz |
| Pulse Width Low | tCLKL | 7 | | | ns |
| Pulse Width High | tCLKH | 7 | | | ns |
| **LRCK Frequency** (Note 18) | | | | | |
| Normal Speed Mode (DFS = "L") | fsn | 30 | 44.1 | 54 | kHz |
| Double Speed Mode (DFS = "H") | fsd | 60 | 88.2 | 108 | kHz |
| Duty Cycle | Duty | 45 | | 55 | % |
| **Serial Interface Timing** | | | | | |
| BICK Period | tBCK | 140 | | | ns |
| BICK Pulse Width Low | tBCKL | 60 | | | ns |
| Pulse Width High | tBCKH | 60 | | | ns |
| BICK "↑" to LRCK Edge (Note 19) | tBLR | 20 | | | ns |
| LRCK Edge to BICK "↑" (Note 19) | tLRB | 20 | | | ns |
| SDATA Hold Time | tSDH | 20 | | | ns |
| SDATA Setup Time | tSDS | 20 | | | ns |
| **Control Interface Timing** | | | | | |
| CCLK Period | tCCK | 200 | | | ns |
| CCLK Pulse Width Low | tCCKL | 80 | | | ns |
| Pulse Width High | tCCKH | 80 | | | ns |
| CDTI Setup Time | tCDS | 50 | | | ns |
| CDTI Hold Time | tCDH | 50 | | | ns |
| CSN High Time | tCSW | 150 | | | ns |
| CSN "↓" to CCLK "↑" | tCSS | 50 | | | ns |
| CCLK "↑" to CSN "↑" | tCSH | 50 | | | ns |
| **Reset Timing** | | | | | |
| PDN Pulse Width (Note 20) | tPW | 150 | | | ns |

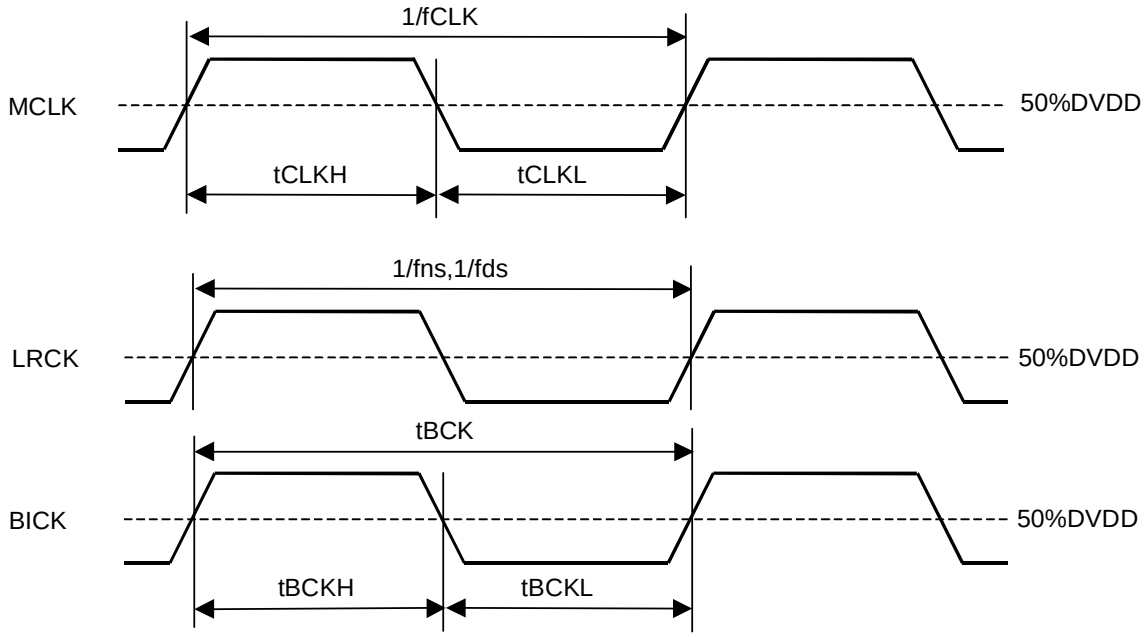
Notes: 17. **For Double Speed mode please see Appendix A for relationship of MCLK and BCLK/LRCK.**

18. When the normal and double speed modes are switched, AK4393 should be reset by PDN pin or RSTN bit.

19. BICK rising edge must not occur at the same time as LRCK edge.

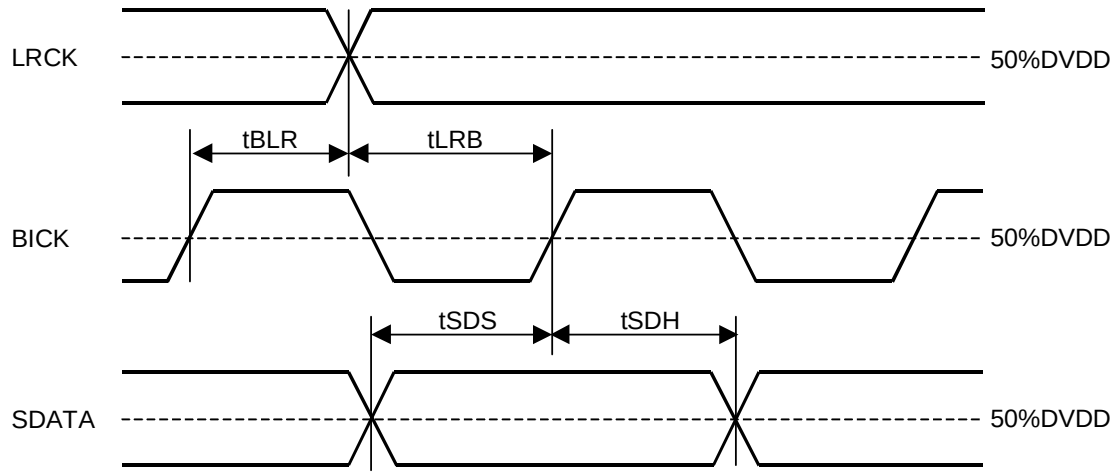
20. The AK4393 can be reset by bringing PDN "L" to "H".
When the states of CKS2-0 or DFS change, the AK4393 should be reset by PDN pin or RSTN bit.

■ **Timing Diagram**

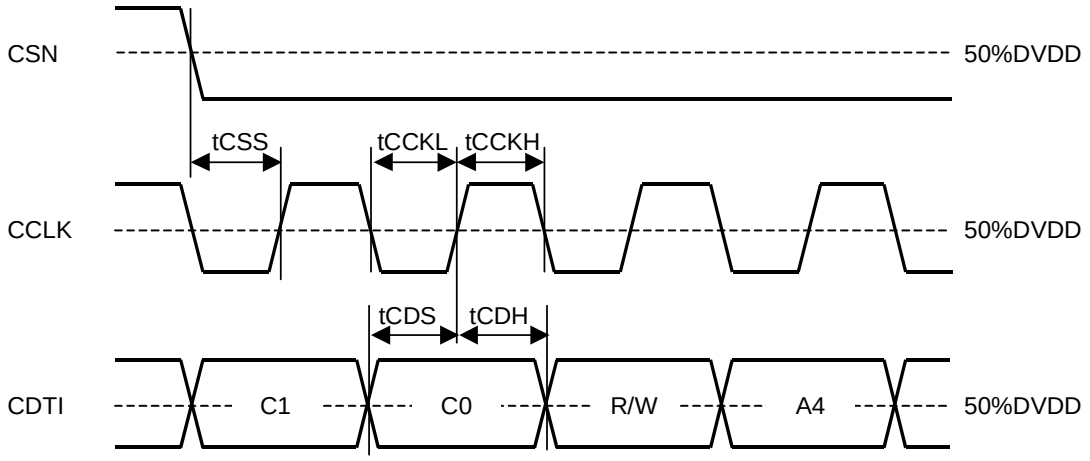



Clock Timing

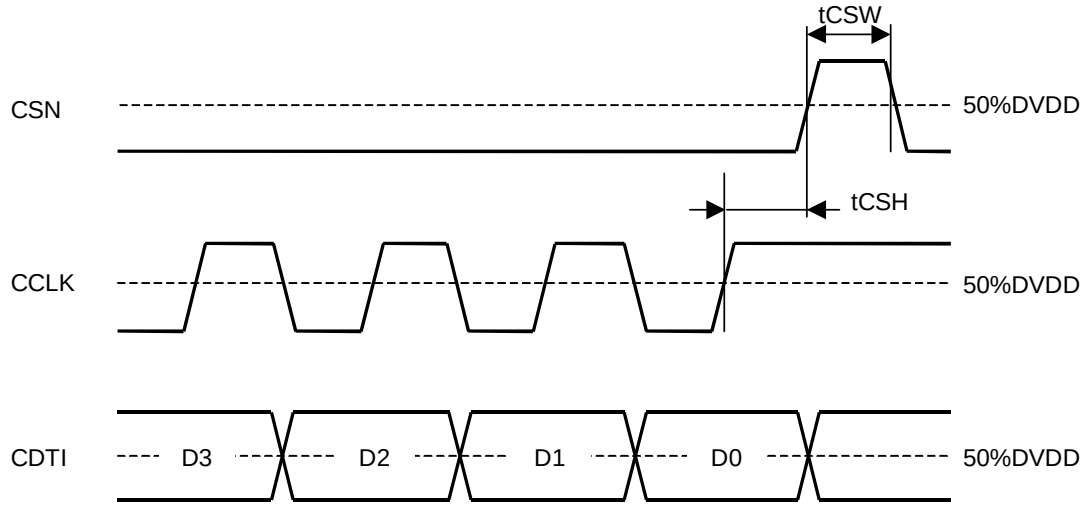
**For Double Speed mode timing please see Appendix A for relationship of MCLK and BCLK/LRCK.**



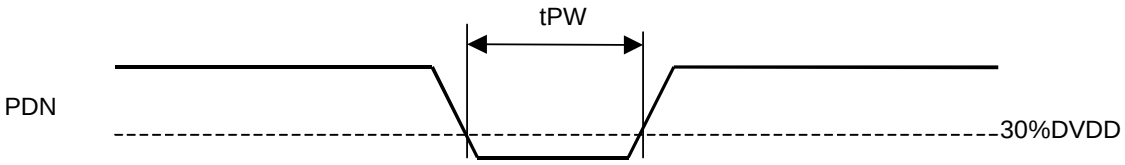

Audio Interface Timing




WRITE Command Input Timing




WRITE Data Input Timing




Power-down Timing

## OPERATION OVERVIEW

### ■ System Clock

The external clocks, which are required to operate the AK4393, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. **However, in Double Speed Mode, the phase relationship between MCLK and LRCK/BICK is limited. (Refer to Appendix A).** The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. The sampling speed is set by DFS (Table 1). The sampling rate (LRCK), CKS0/1/2 and DFS determine the frequency of MCLK (Table 2).

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4393 is in normal operation mode (PDN = "H"). If these clocks are not provided, the AK4393 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4393 should be in the power-down mode (PDN = "L") or in the reset mode (RSTN = "0"). After exiting reset at power-up etc., the AK4393 is in power-down mode until MCLK and LRCK are input.

| DFS | Sampling Rate (fs) | | |
|---|---|---|---|
| 0 | Normal Speed Mode | 30kHz~54kHz | Default |
| 1 | Double Speed Mode | 60kHz~108kHz | |

Table 1. Sampling Speed

| Mode | CKS2 | CKS1 | CKS0 | Normal | Double | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 256fs | 128fs | Default |
| 1 | 0 | 0 | 1 | 256fs | 256fs | |
| 2 | 0 | 1 | 0 | 384fs | 192fs | |
| 3 | 0 | 1 | 1 | 384fs | 384fs | |
| 4 | 1 | 0 | 0 | 512fs | 256fs | |
| 5 | 1 | 0 | 1 | 512fs | N/A | |
| 6 | 1 | 1 | 0 | 768fs | 384fs | |
| 7 | 1 | 1 | 1 | 768fs | N/A | |

Table 2. System Clocks

| LRCK | MCLK | | | | BICK |
|---|---|---|---|---|---|
| fs | 256fs | 384fs | 512fs | 768fs | 64fs |
| 32.0kHz | 8.1920MHz | 12.2880MHz | 16.3840MHz | 24.5760MHz | 2.0480MHz |
| 44.1kHz | 11.2896MHz | 16.9344MHz | 22.5792MHz | 33.8688MHz | 2.8224MHz |
| 48.0kHz | 12.2880MHz | 18.4320MHz | 24.5760MHz | 36.8640MHz | 3.0720MHz |

Table 3. System clock example (Normal Speed Mode)

| LRCK | MCLK | | | | BICK |
|---|---|---|---|---|---|
| fs | 128fs | 192fs | 256fs | 384fs | 64fs |
| 88.2kHz | 11.2896MHz | 16.9344MHz | 22.5792MHz | 33.8688MHz | 5.6448MHz |
| 96.0kHz | 12.2880MHz | 18.4320MHz | 24.5760MHz | 36.8640MHz | 6.1440MHz |

Table 4. System clock example (Double Speed Mode)

## ■ Audio Serial Interface Format

Data is shifted in via the SDATA pin using BICK and LRCK inputs. Five data formats are supported and selected by the DIF0-2 as shown in Table 5. In all formats the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20 and 16 MSB justified formats by zeroing the unused LSBs.

| Mode | DIF2 | DIF1 | DIF0 | Mode | BICK | Figure |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0: 16bit LSB Justified | ≥32fs | Figure 1 |
| 1 | 0 | 0 | 1 | 1: 20bit LSB Justified | ≥40fs | Figure 2 |
| 2 | 0 | 1 | 0 | 2: 24bit MSB Justified | ≥48fs | Figure 3 |
| 3 | 0 | 1 | 1 | 3: $I^2S$ Compatible | ≥48fs | Figure 4 |
| 4 | 1 | 0 | 0 | 4: 24bit LSB Justified | ≥48fs | Figure 2 |

Table 5. Audio Data Formats

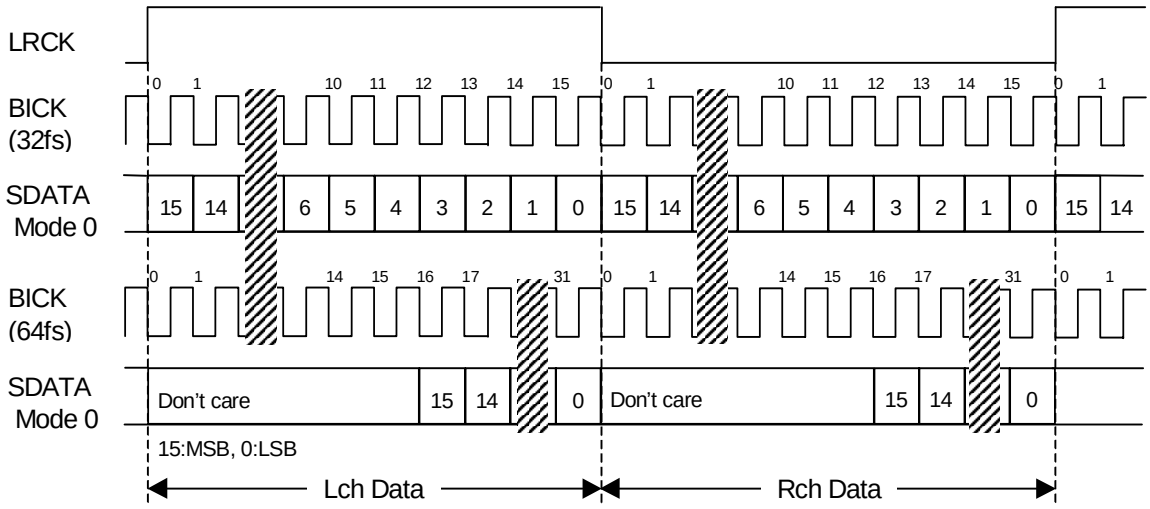



Figure 1. Mode 0 Timing

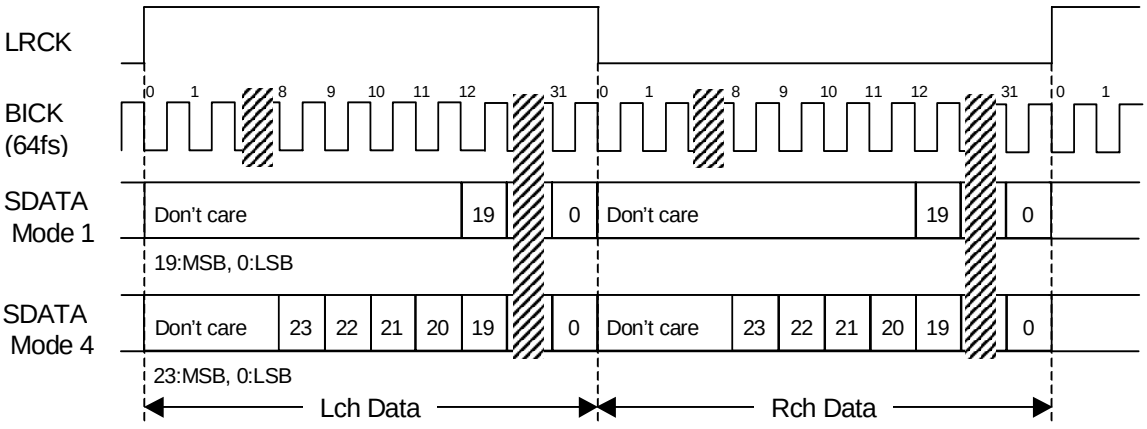



Figure 2. Mode 1,4 Timing

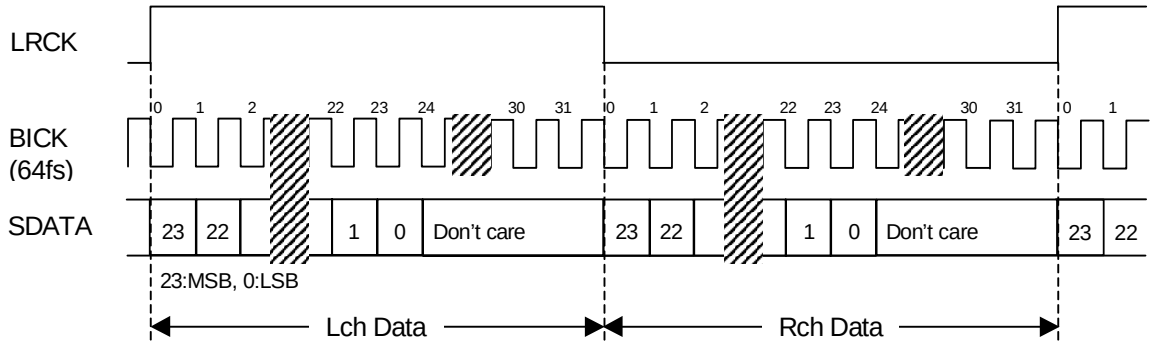



Figure 3. Mode 2 Timing

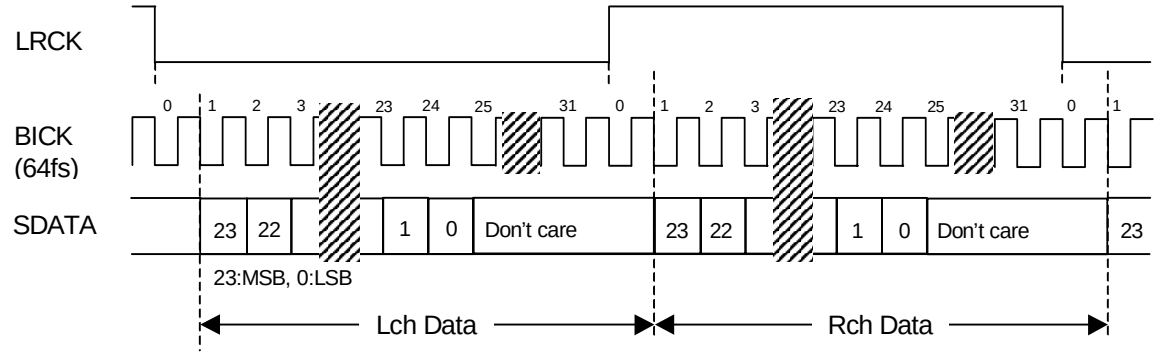



Figure 4. Mode 3 Timing

## ■ De-emphasis filter

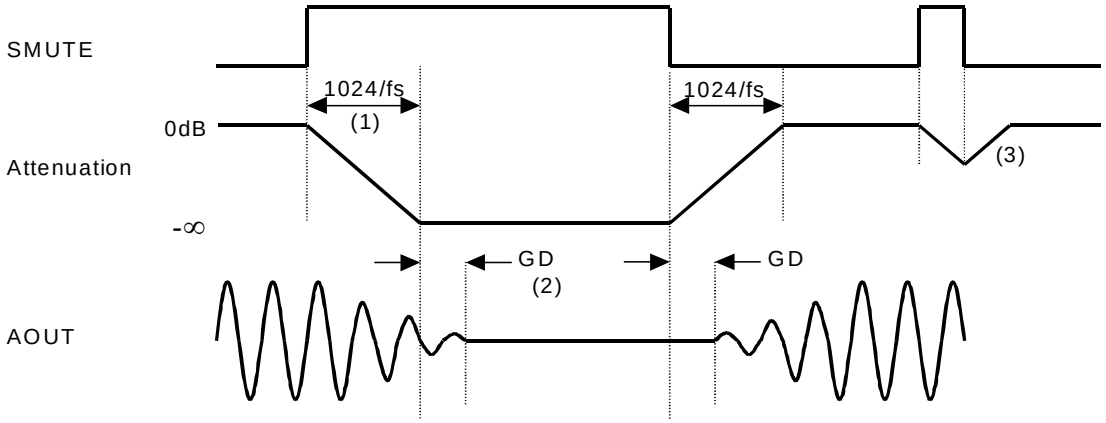
A digital de-emphasis filter is available for 32, 44.1, 48 or 96kHz sampling rates (tc = 50/15μs) and is enabled or disabled with the DEM0, DEM1 and DFS input pins.

| DEM1 | DEM0 | DFS | Mode | |
|---|---|---|---|---|
| 0 | 0 | 0 | 44.1kHz | Default |
| 0 | 1 | 0 | OFF | |
| 1 | 0 | 0 | 48kHz | |
| 1 | 1 | 0 | 32kHz | |
| 0 | 0 | 1 | OFF | |
| 0 | 1 | 1 | OFF | |
| 1 | 0 | 1 | 96kHz | |
| 1 | 1 | 1 | OFF | |

Table 6. De-emphasis filter control

## ■ Soft mute operation

Soft mute operation is performed at digital domain. When SMUTE goes to "H", the output signal is attenuated by -∞ during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.




Notes:

(1) The output signal is attenuated by -∞ during 1024 LRCK cycles (1024/fs).
(2) Analog output corresponding to digital input has the group delay (GD).
(3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

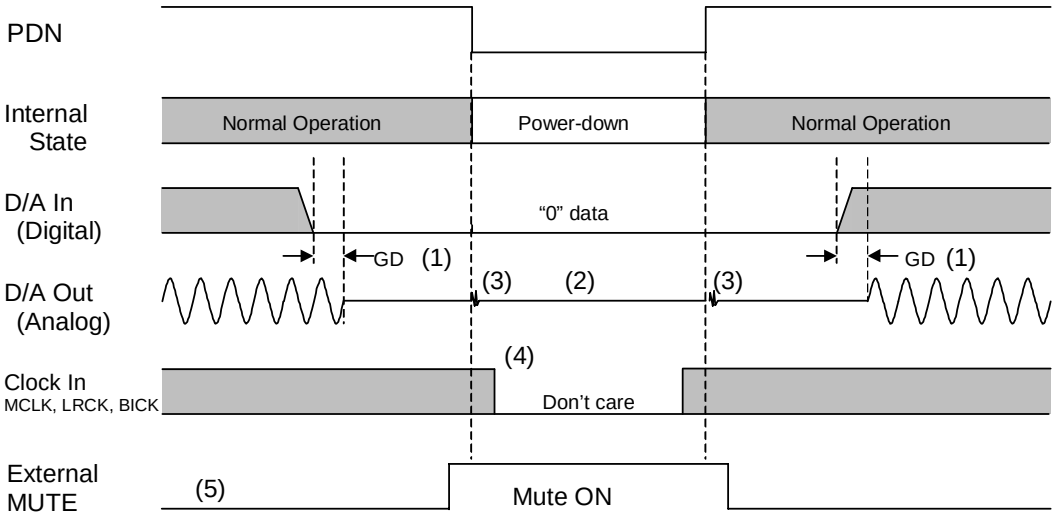
Figure 5. Soft mute operation

## ■ System Reset

The AK4393 should be reset once by bringing PDN = "L" upon power-up. The AK4393 is powered up and the internal timing starts clocking by LRCK "↑" after exiting reset and power down state by MCLK. The AK4393 is in the power-down mode until MCLK and LRCK are input.

## ■ Power-Down

The AK4393 is placed in the power-down mode by bringing PDN pin "L" and the anlog outputs are floating (Hi-Z). Figure 6 shows an example of the system timing at the power-down and power-up.




Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are floating (Hi -Z) at the power-down mode.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = "L").
(5) Please mute the analog output externally if the click noise (3) influences system application. The timing example is shown in this figure.

Figure 6. Power-down/up sequence example

## ■ Click Noise from analog output

Click noise occurs from analog output in the following cases.

1) When switching de-emphasis mode by DEM0, DEM1 and DFS pins,
2) When switching serial data mode by DIF0, DIF1 and DIF2 pins,
3) When going and exiting power down mode by PDN pin,
4) When switching normal speed and double speed by DFS pin,

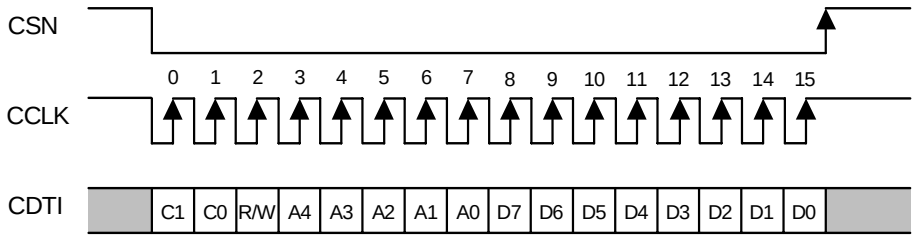
However in case of 1) & 2), If the input data is "0" or the soft mute is enabled (after 1024 LRCK cycles from SMUTE = "H"), no click noise occur except for switching DFS pin.

## ■ Mode Control Interface

Pins (parallel control mode) or registers (serial control mode) can control each functions of the AK4393. For DIF2-0, CKS2-0 and DFS, the setting of pin and register are "ORed" internally. So, even serial control mode, pin setting can also control these functions.

The serial control interface is enabled by the P/S pin = "L". In this mode, pin setting must be all "L". Internal registers may be written by 3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2bits, C1/0; fixed to "01"), Read/Write (1bit; fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). The AK4393 latches the data on the rising edge of CCLK, so data should be clocked in on the falling edge. The writing of data becomes valid by CSN "↑". The clock speed of CCLK is 5MHz(max). The CSN and CCLK must be fixed to "H" when the register does not be accessed.

PDN = "L" resets the registers to their default values. When the state of P/S pin is changed, the AK4393 should be reset by PDN = "L". In serial mode, the internal timing circuit is reset by RSTN bit, but the registers are not initialized.




C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 7. Control I/F Timing

*The AK4393 does not support the read command and chip address. C1/0 and R/W are fixed to "011"
*When the AK4393 is in the power down mode (PDN = "L") or the MCLK is not provided, writing into the control register is inhibited.
*For setting the registers, the following sequence is recommended.

- Control 1 register
  (1) Writing RSTN = "0" and other bits (D6-D1) to the register at the same time.
  (2) Writing RSTN = "1" to the register. The other bits are no change.
- Control 2 register
  This writing sequence has no limitation like control 1 register.

*When RSTN = "0", the click noise is output from AOUT pins.
*If the mode setting is done without setting RSTN = "0", large noise may be output from AOUT pins. (Especially when CKS0/1/2 are changed.)

## ■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Control 1 | 0 | CKS2 | CKS1 | CKS0 | DIF2 | DIF1 | DIF0 | RSTN |
| 01H | Control 2 | 0 | 0 | 0 | 0 | DFS | DEM1 | DEM0 | SMUTE |
| 02H | Test | TEST7 | TEST6 | TEST5 | TEST4 | TEST3 | TEST2 | TEST1 | TEST0 |

Notes:

For addresses from 03H to 1FH, data must not be written.

When PDN pin goes to "L", the registers are initialized to their default values. When RSTN bit goes to "0", the only internal timing is reset and the registers are not initialized to their default values. DIF2-0, CKS2-0 and DFS bits are ORed with pins respectively.

## ■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00H | Control 1 | 0 | CKS2 | CKS1 | CKS0 | DIF2 | DIF1 | DIF0 | RSTN |
| default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

RSTN: Internal timing reset

0: Reset. All registers are not initialized.

1: Normal Operation

When the states of CKS2-0 or DFS change, the AK4393 should be reset by PDN pin or RSTN bit.

DIF2-0: Audio data interface modes (see Table 5)

Initial: "000", Mode 0

Register bits are ORed with DIF2-0 pins if P/S = "L".

CKS2-0: Master Clock Frequency Select (see Table 2)

Initial: "000", Mode 0

Register bits are ORed with CKS2-0 pins if P/S = "L".

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 01H | Control 2 | 0 | 0 | 0 | 0 | DFS | DEM1 | DEM0 | SMUTE |
| default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SMUTE: Soft Mute Enable

0: Normal operation

1: DAC outputs soft-muted

DEM1-0: De-emphasis response (see Table 6)

Initial: "00", 44.1kHz

DFS: Sampling speed control (see Table 1)

0: Normal speed

1: Double speed

Register bit is ORed with DFS pin if P/S = "L".

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 02H | Test | TEST7 | TEST6 | TEST5 | TEST4 | TEST3 | TEST2 | TEST1 | TEST0 |
| default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TEST7-0: Test mode. Do not write any data to 02H.

## SYSTEM DESIGN

Figure 8 and 9 show the system connection diagram. An evaluation board (AKD4393) is available which demonstrates the optimum layout, power supply arrangements and measurement results.

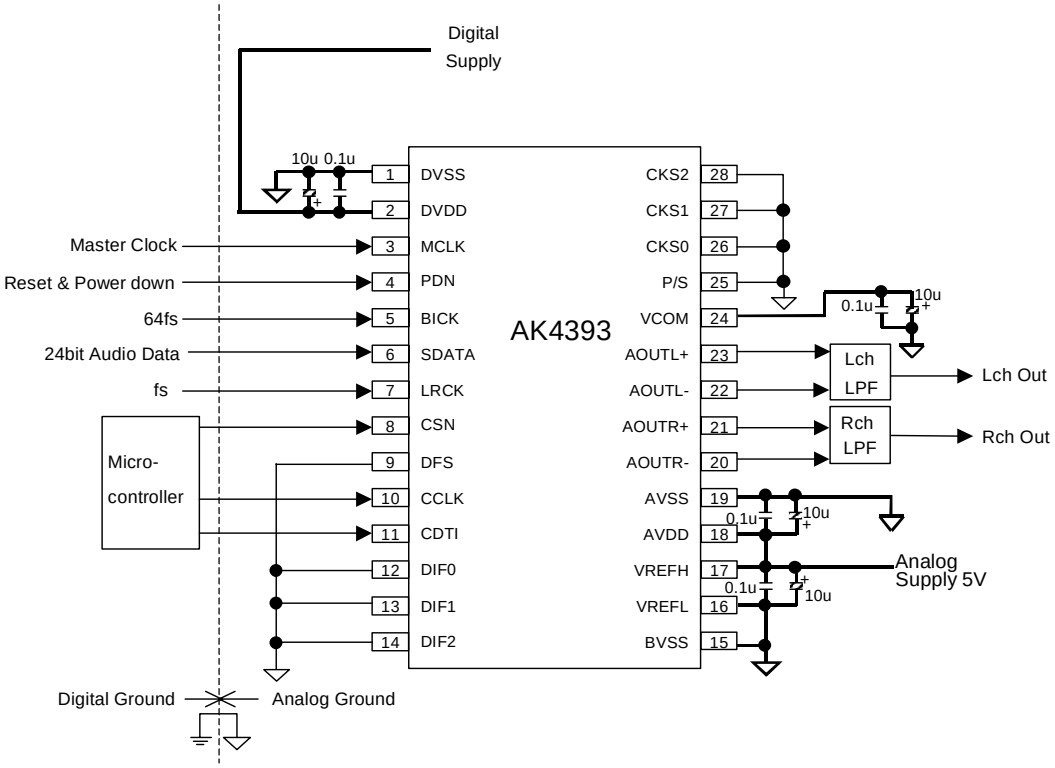



Figure 8. Typical Connection Diagram (Serial mode)

Notes:

- LRCK = fs, BICK = 64fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS, BVSS and DVSS must be connected to the same analog ground plane.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down/pull-up pins should not be left floating.

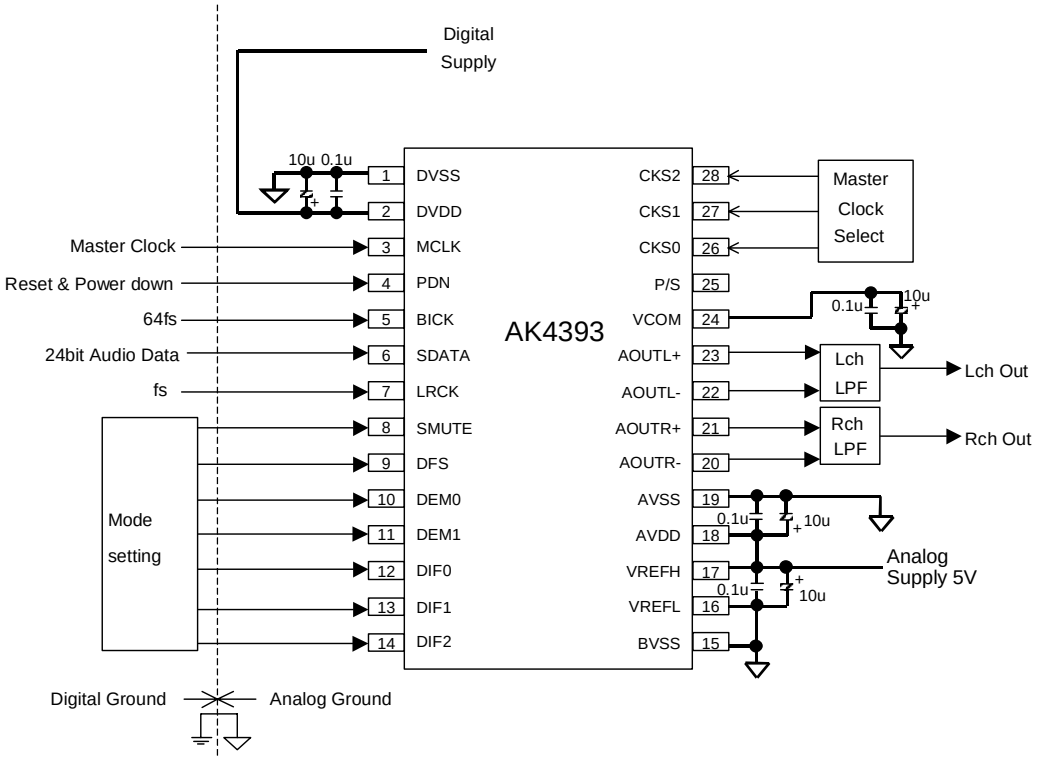



Figure 9. Typical Connection Diagram (Parallel mode)

Notes:

- LRCK = fs, BICK = 64fs.
- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- AVSS, BVSS and DVSS must be connected to the same analog ground plane.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down/pull-up pins should not be left floating.

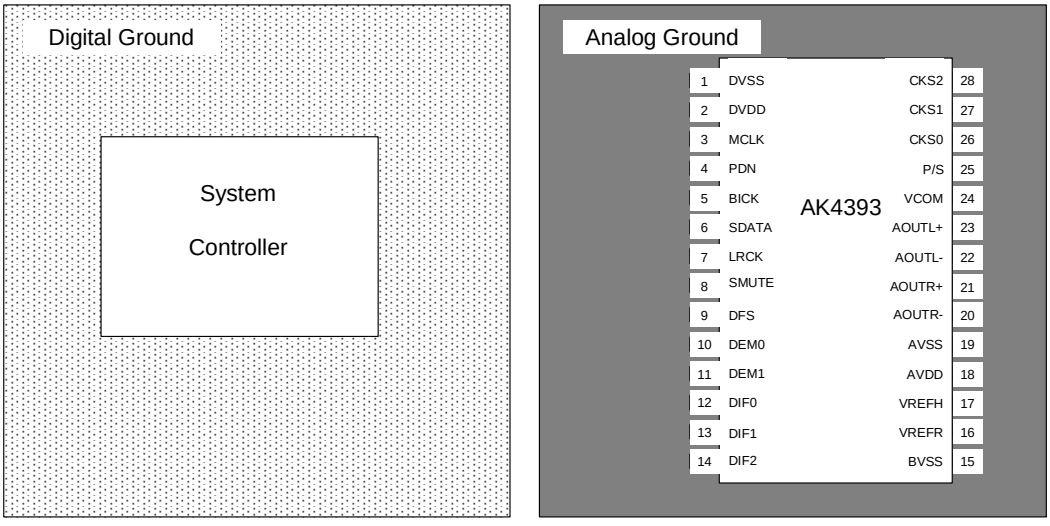



Figure 10. Ground Layout

## 1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from digital supply in system. If AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS, BVSS and DVSS must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible.

## 2. Voltage Reference

The differential Voltage between VREFH and VREFL set the analog output range. VREFH pin is normally connected to AVDD and VREFL pin is normally connected to AVSS. VREFH and VREFL should be connected with a 0.1µF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 10µF parallel with a 0.1µF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREFH, VREFL and VCOM pins in order to avoid unwanted coupling into the AK4393.

## 3. Analog Outputs

The analog outputs are full differential outputs and 2.4Vpp (typ@VREF=5V) centered around VCOM. The differential outputs are summed externally, $V_{AOUT}$ = (AOUT+) - (AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is 4.8Vpp (typ@VREF=5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage ($V_{AOUT}$) is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal $V_{AOUT}$ is 0V for 000000H(@24bit).

The internal switched-capacitor filters attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

Figure 11 shows an example of external LPF circuit summing the differential outputs by an op-amp.
Figure 12 shows an example of differential outputs and LPF circuit example by three op-amps.

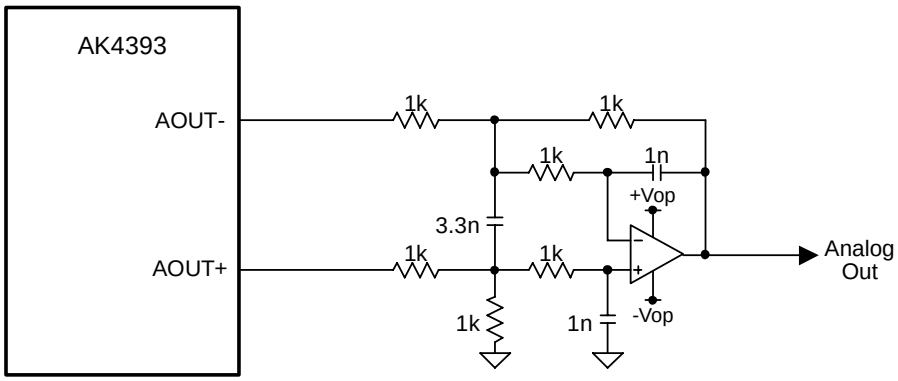



Figure 11. External LPF Circuit Example 1

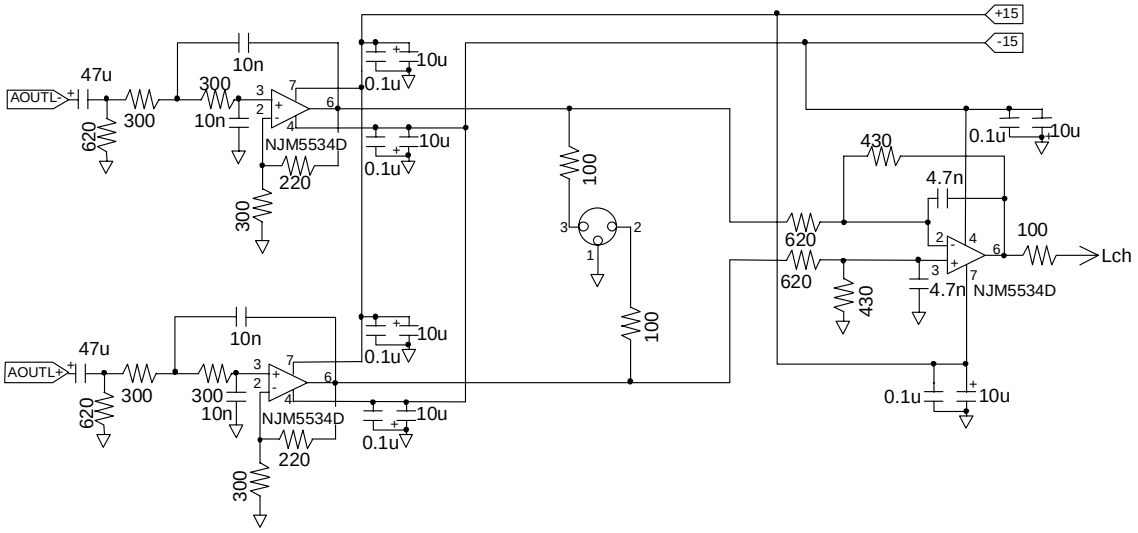
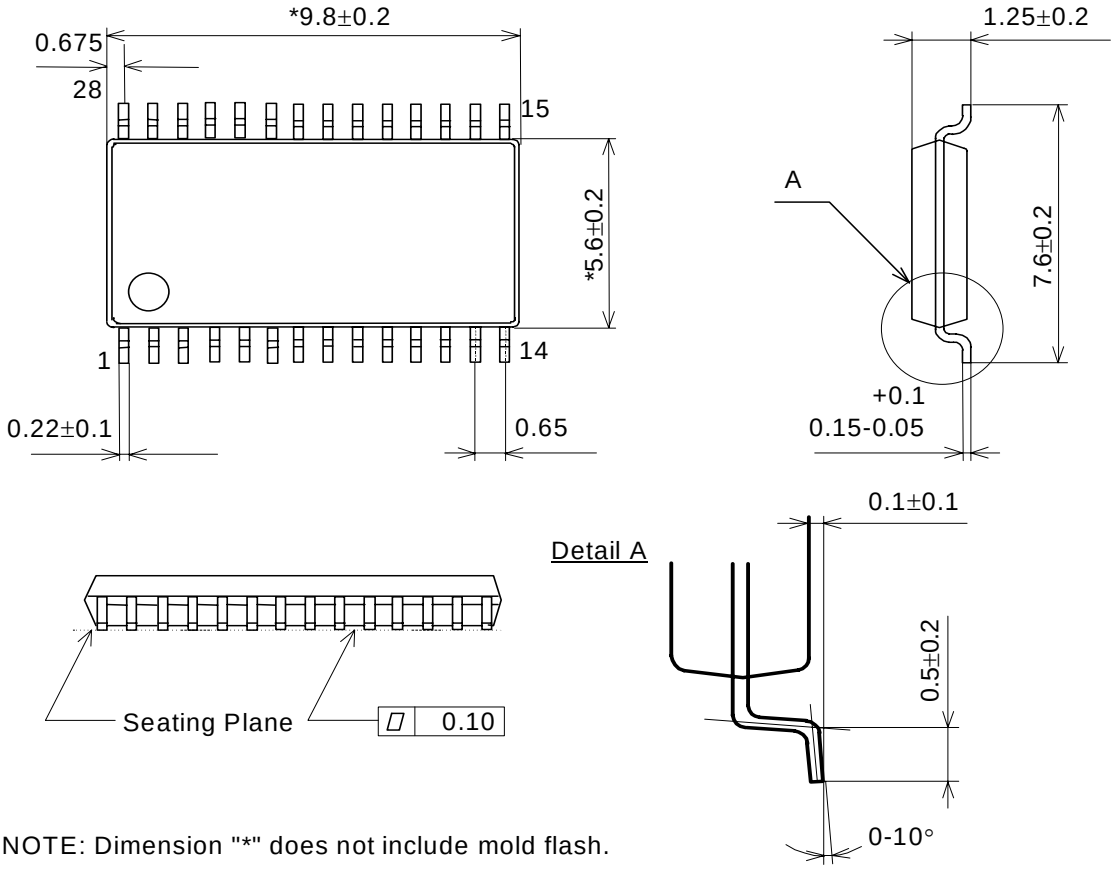



Figure 12. External LPF Circuit Example 2

## PACKAGE

28pin VSOP (Unit: mm)

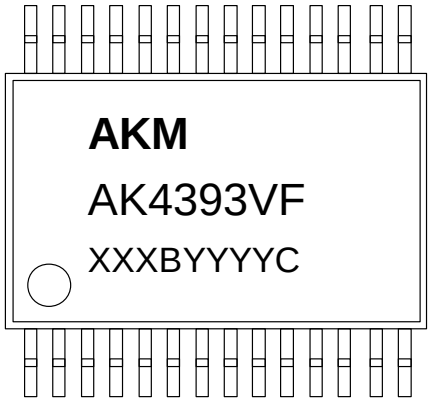



NOTE: Dimension "*" does not include mold flash.

■ **Material & Lead finish**

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate

## MARKING




XXXXBYYYYC data code identifier

XXXB: Lot number (X : Digit number, B : Alpha character )
YYYYC: Assembly date (Y : Digit number C : Alpha character)

## Appendix A

In Double Speed Mode, the phase relationship between MCLK and LRCK/BICK is limited (Table 7). If the phase relationship happens during this prohibited period, it is possible to occur the inverse of output channel. The phase relationship must be set to avoid the prohibited period when the AK4393 operates at Double Speed Mode. The prohibited period is specified by the combination of digital power supply voltage (DVDD), MCLK frequency and audio data format (Table 5). When the audio data formats are 16/20/24bit LSB Justified (Mode 0,1,4) and 24bit MSB Justified (Mode 2), the phase relationship (tLRM: Figure 11) between the rising edge of LRCK and the rising edge of MCLK has the prohibited period of min to max in Table 7. In case of $I^2S$ Compatible (Mode 3), the relationship between the falling edge of BICK and the rising edge of MCLK has the prohibited period (tBCM: Figure 12)

| Sampling Mode | Digital Power Supply, DVDD | MCLK Frequency | Mode Setting | | | | Prohibited Period | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | CKS2 | CKS1 | CKS0 | DFS | min | max | |
| Double Speed | 3.0 to 5.25V | 128fs | 0 | 0 | 0 | 1 | 0.4 | 1.7 | ns |
| Double Speed | 3.0 to 5.25V | 192fs | 0 | 1 | 0 | 1 | -0.5 | 0.8 | ns |
| Double Speed | 3.0 to 5.25V | 256fs | 0 | 0 | 1 | 1 | -0.7 | 0.7 | ns |
| Double Speed | 3.0 to 5.25V | 256fs | 1 | 0 | 0 | 1 | -0.7 | 0.7 | ns |
| Double Speed | 3.0 to 5.25V | 384fs | 0 | 1 | 1 | 1 | -1.7 | -0.3 | ns |
| Double Speed | 3.0 to 5.25V | 384fs | 1 | 1 | 0 | 1 | -1.7 | -0.3 | ns |
| Double Speed | 4.75 to 5.25V | 128fs | 0 | 0 | 0 | 1 | 0.8 | 1.5 | ns |
| Double Speed | 4.75 to 5.25V | 192fs | 0 | 1 | 0 | 1 | -0.2 | 0.5 | ns |
| Double Speed | 4.75 to 5.25V | 256fs | 0 | 0 | 1 | 1 | -0.3 | 0.4 | ns |
| Double Speed | 4.75 to 5.25V | 256fs | 1 | 0 | 0 | 1 | -0.3 | 0.4 | ns |
| Double Speed | 4.75 to 5.25V | 384fs | 0 | 1 | 1 | 1 | -1.0 | -0.3 | ns |
| Double Speed | 4.75 to 5.25V | 384fs | 1 | 1 | 0 | 1 | -1.0 | -0.3 | ns |

Table **7**. Prohibited Period

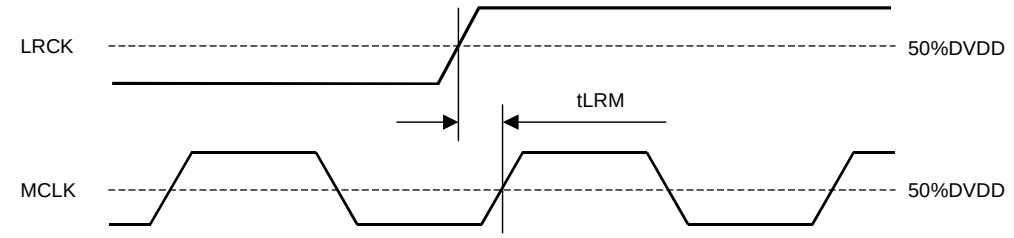



Figure 11. 16/20/24bit LSB Justified, 24bit MSB Justified

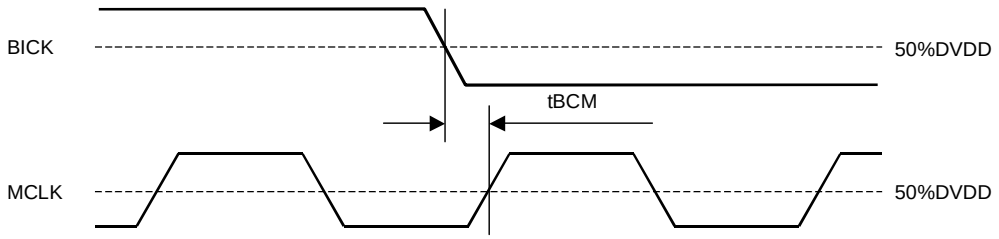



Figure 12. $I^2S$ Compatible